REMARKS

Claims 1-20 are currently pending in this application. Applicant has amended claims 1, 8 and 15. Applicant has not added or canceled any claims. Thus, claims 1-20 remain pending.

The Office Action rejects claims 1-7 and 15-20 under 35 U.S.C. § 112. Although applicant respectfully traverses, applicant has nevertheless amended these claims to expedite prosecution by substituting the term "substantially" with "at least approximately," and requests reconsideration.

The Office Action rejects claims 1-6, 8-13, and 15-19 under 35 U.S.C. § 103(a) over the combination of U.S. Patent No. 6,754,899 ("Stoye"), U.S. Patent No. 6,438,672 ("Fischer"), and U.S. Patent Pub. No. 20030033490 ("Gappisch"). The Office Action rejects claims 7, 14, and 20 under 35 U.S.C. § 103(a) over the combination of Stoye, Fischer, Gappisch, and U.S. Patent Pub. No. 20020098886. Applicant respectfully traverses.

Claims 1-7 recite "the external memory unit includes a data segment configured to store flow control parameters and numerical arithmetic of the microprocessor unit that were originally stored in the internal memory unit, wherein a storage capacity of the data segment included in the external memory unit is at least approximately equal to a storage capacity of the internal memory unit." According to the Office Action, Fischer discloses this feature at 6:45-7:6. The cited passage discusses loading memory addresses upon startup and not anything remotely similar to this claimed feature.

Fischer is directed to a memory aliasing technique. The technique stores repeatedly referenced information in a spare memory (e.g., in a fast memory; also known as cache memory) and, when the stored information is accessed, the technique redirects the processor to load the accessed information from the spare memory.

Applicant's technology is directed to enabling a chip to access data that is stored in memory that is external to the chip, thereby reducing manufacturing cost for the chip. Because applicant's technology stores in the external memory "flow control parameters and numerical arithmetic of the microprocessor unit that were originally stored in the internal memory," it employs external memory that has storage capacity "at least approximately equal to a storage capacity of the internal memory unit."

In complete contrast, Fischer's technique has absolutely no need for a spare memory storage capacity that is "at least approximately equal to a storage capacity of the internal memory unit" because spare (or cache) memory holds "a small subset of data stored in the main memory. The processor needs only a certain (sic, a) small amount of the data in the main memory to execute individual instructions for a particular application." (Fischer, 1:53-54.) In Fischer, the memory aliasing module intercepts the data path between the addressable circuits (e.g., memory) and the processor and, when the most significant bit (MSB) of the address is high (e.g., 1), Fischer's technique redirects the memory to the spare memory. (Fischer, 8:7-19.) Because the most significant bit of the address is used to determine whether or not the spare memory is to be referenced, the capacity of the spare memory can be no more than half the capacity of the main memory. Thus, Fischer teaches away because the external (spare) memory used by Fischer's technique must be significantly smaller than its main memory. Moreover, modifying Fischer's technique to use external memory that is the same size as the internal memory would destroy how Fischer's technique operates.

The Office Action points to no other reference as teaching or suggesting this feature. Accordingly, claims 1-7 patentably define over the references, both alone and in combination. Applicant respectfully requests reconsideration.

Claims 8-14 now recite "wherein a capacity of the external memory unit is at least approximately equal to a capacity of the internal memory unit." As stated above, Fischer not only fails to teach or suggest this feature, it teaches away. Accordingly,

claims 8-14 patentably define over the references, both alone and in combination. Applicant respectfully requests reconsideration.

Claims 15-20 recite "a storage capacity of the data segment is at least approximately equal to a storage capacity of the internal memory unit." As stated above, Fischer not only fails to teach or suggest this feature, it teaches away. Accordingly, claims 15-20 patentably define over the references, both alone and in combination.

In view of the above amendment, applicant believes the pending application is in condition for allowance. The claims each recite a novel combination of elements that is neither taught nor suggested by the applied references and so cannot be properly rejected under 35 U.S.C. § 102(b) or 35 U.S.C. § 103(a). Applicant does not concede any rejection not specifically responded to and reserves its rights to respond to such rejections later.

Based on these amendments and remarks, applicant respectfully requests early allowance of this application. If the Examiner has any questions or believes a telephone conference would expedite prosecution of this application, the Examiner is encouraged to call the undersigned at (206) 359-6478.

Fees due with this response will be paid via EFT Account (as shown on the accompanying transmittal). The Director is hereby authorized to charge any deficiencies in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to Deposit Account No. 50-0665 under Order No. 320528721US, from which the undersigned is authorized to draw.

Respectfully submitted,
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